PULSED POWER PERFORMANCE OF GaAs FETS AT X-BAND

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ABSTRACT

The pulsed operation of X-band amplifiers using 4.8 mm power FETs resulted in a nominal output power improvement of 2 dB when operated at elevated drain voltages of up to 18 volts. An ouptut power of 6 W peak with 6 dB gain at 10 GHz was obtained from a balanced amplifier.

INTRODUCTION

The growing requirements for high power generation at microwave frequencies using GaAs FETs has motivated the development of devices with gate peripheries in excess of one mm. Large periphery devices, consisting of a parallel interconnection of many device cells, exhibit low input and output impedances which require special matching techniques to achieve optimum performance. The incorporation of matching networks directly on the device carrier has been shown to improve power gain performance by minimizing the loss between the device and the circuit.(1) The source connection requirements associated with multicell devices give rise to a large common-lead source inductance which degrades gain and induces spurious oscillations. The use of via hole source connections has yielded stable device operation, free of the high frequency oscillations commonly observed in conventionally wire-bonded transistors.(1)

The output power of large periphery devices is further limited by gate-drain breakdown voltage and channel operating temperature. The continued development of GaAs power FETs at Raytheon has resulted in processing techniques which have significantly increased the device breakdown voltage. Pulsed operation is currently being investigated for radar applications as a mode of operation which will reduce channel temperature through reduced power dissipation. Previous results (2,3) have shown that drain pulsing of power FETs yields a significant improvement in device output power. Recent results, at Raytheon, using gate pulsing of 4.8 mm devices, indicate that an improvement of more than 2 dB in output power can be obtained when operating the devices at elevated drain voltages.

DEVICE AND AMPLIFIER DESIGN

The device used in this investigation, a Raytheon RPX 4320, has a total gate periphery of 4.8 mm and is divided into four cells. Each cell has eight gates in parallel and the unit gate width is 150 μm. The device contains an Al gate with a Ti/Pt/Au transition to an Au bonding pad. Aluminum gates with this type of transition, have an established record of high reliability(4). Each source pad is connected to ground using a via-hole connection through the GaAs wafer.

Small signal S-parameters of many devices were measured at 10 GHz and a typical set is shown below. These S-parameters are considered to represent an adequate approximation for large-signal amplifier design.

$$S_{11} = 0.97 \angle +175°$$
$$S_{12} = 0.014 \angle +36°$$
$$S_{21} = 0.31 \angle +7°$$
$$S_{22} = 0.92 \angle -153°$$

The small magnitude of S_{12} indicates that for the purpose of designing the input and output matching networks the device may be considered to be unilateral. Furthermore, the large magnitudes of S_{11} and S_{22} (> 0.9) are indicative of the low input and output impedances of large periphery devices.

Simple, two section, quarter-wave transformer matching networks were designed to match the input and output impedances of the 4.8 mm device to 50 ohms. Both input and output networks contained a low impedance 15 ohm transformer adjacent to the device and were followed by a 90 ohm transformer. A network of this design was capable of providing reasonable match to device impedances of less than 2 ohms. The 15 ohm transformers were realized on 25 mil alumina substrates and were located on the device carrier. The second transformer and associated amplifier bias networks were located on separate substrates adjacent to the device carrier.

EXPERIMENTAL RESULTS

In order to evaluate the effect of pulsed operation on power gain performance, several single stage amplifiers were assembled using 4.8 mm devices from a number of different wafers. Each amplifier was initially tuned for best small signal gain over a five percent bandwidth centered at 10 GHz. In the pulsed mode, a gate waveform was fed to the device which biased the device beyond pinch-off during the interpulse period. The measurement of peak power was based upon the calibration of a detector output voltage corresponding to the amplifier input power. This detected voltage was referenced to a line on the oscilloscope display and for each measurement of amplifier output power, additional attenuation was introduced before the detector so as to align the peak of the amplifier output to the calibrated reference level. The peak output power was then calculated as the sum of the added attenuation and the known RF input power. The peak output power was also monitored using a peak power meter.

The output power performance as a function of the applied drain voltage is shown in Figure 1. It was found that in the CW mode (i. e., continuous gate bias), with an input power of 27 dBm the output power saturated at a level of 32.2 dBm for a drain voltage of 15 volts. The amplifier was then pulsed by biasing the gate beyond pinch-off (-5 V) during the interpulse period. For a peak input power of 27 dBm, a pulse width of 2 μsec and a duty factor of 20 percent, the amplifier output power was observed to saturate at a level of 34.2 dBm with 18 volts applied to the drain. At each drain voltage, in both the CW and pulsed modes, the device gate voltage was adjusted to provide optimum output power. These results indicate that the useful range of drain voltage is extended under pulsed conditions and results in a 2 dB improvement in power gain.

	CW	PULSED
(V_{DS}) SAT	15V	18V
(P_{OUT}) SAT	32.2 dBm	34.2 dBm

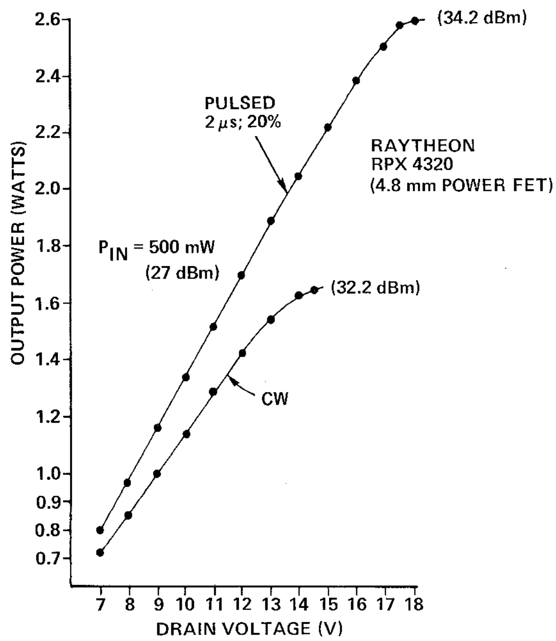

Figure 1 - Output Power (Watts) versus Drain Voltage (Volts)

These experiments were repeated for several amplifiers and the performance data is tabulated below. These measurements indicate an average power gain improvement of 1.97 dB. Furthermore, the drain voltage at which the output power saturates is an average of 3.7 volts higher in the pulsed mode.

Amplifier No.	CW Performance Pin = 500 mW		Pulsed Performance Pin = 500 mW		Power Gain Improvement (dB)
	$(V_{DS})_{sat}$ (V)	$(P_{out})_{sat}$ (W)	$(V_{DS})_{sat}$ (V)	$(P_{out})_{sat}$ (W)	
1	15	1.66	18	2.59	1.9
2	11	1.13	16	1.83	2.1
3	15	1.75	16	2.68	1.8
4	14	1.19	19	1.81	1.8
5	10	1.24	16	2.12	2.3
6	11	1.45	13	2.24	1.9

An additional amplifier was tested as described above at an input power level of 1.6 watts and a comparison of pulsed and CW operation is shown in Figure 2. In the pulsed mode, the amplifier provided 4.15 watts of output power which is equivalent to 0.87 W/mm. Furthermore, the associated power gain in the pulsed mode was 4 dB which represents a 2.1 dB improvement over CW performance. The power-added efficiency of the pulsed amplifier was 30 percent.

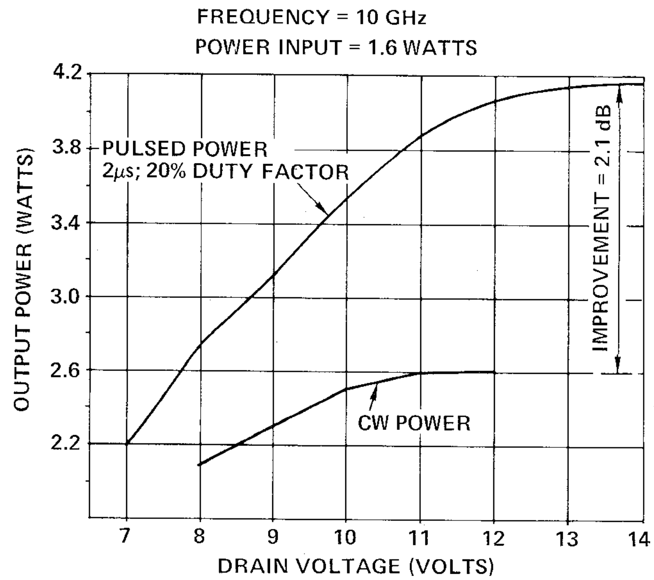

Figure 2 - Comparison of Pulsed and CW Operation of a 4.8 mm GaAs Power FET

Variations in pulse width from 200 nsec to 20 μsec yielded less than a 0.5 dB variation in peak output power at a duty factor of 20 percent. In addition, for a fixed pulsewidth of 2 μsec, a variation in duty factor from five percent to 50 percent resulted in a reduction in pulsed output power of 0.6 dB.

Finally, a balanced amplifier was constructed using two Raytheon RPX 4320 (4.8 mm) devices. The amplifier was operated at room ambient conditions in the pulsed mode. The performance of the amplifier is shown in Figure 3 and indicates an output power of 6 watts peak with an associated power gain of 6 dB at 10 GHz.

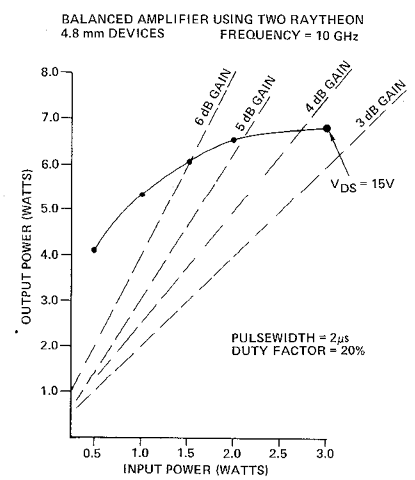

Figure 3 - Output Power (Watts) versus Input Power (Watts) for Pulsed Power FET Amplifier

DISCUSSION

In an earlier paper[5], the CW performance of RPX 4320 type devices was described. Specifically, the dependence of output power on drain bias voltage for devices with high and low gate-drain breakdown voltages was reported. The data is reproduced here in Figure 4. High breakdown devices, with gate-drain breakdown voltages in excess of 30 volts, exhibited a linear dependence of output power on drain bias voltage to significantly higher voltages than low breakdown units. Hence, the observed improvement was attribted to the superior breakdown capability. The amplifiers measured in conjunction with this investigation (see previous table) contained low-breakdown devices with nominal gate-drain breakdown voltages of 15 volts. These low-breakdown devices, when operated in the pulsed mode, exhibited a similar improvement in output power (Figures 1, 2) to that presented in Figure 4. In these cases, the improvements could be attributed to the reduced channel temperature under pulsed operation. In the absence of the previous CW results (Figure 4) the reduced channel temperature might have constituted an adequate explanation, but the striking similarity between the two sets of data suggests that both breakdown and thermal effects are contributing to the improved performance obtained under pulsed operation. Investigation is continuing to determine the contributions of channel temperature and breakdown to the mechanism responsible for the saturation of output power under pulsed conditions.

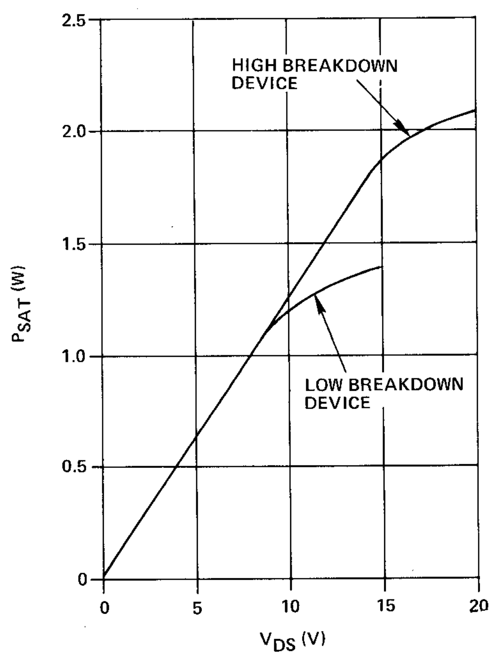

Figure 4 - Saturated Output Power versus Drain Bias Voltage for High and Low Breakdown Voltages

CONCLUSIONS

Pulsed experiments performed on several amplifiers using 4.8 mm devices resulted in a nominal improvement of 2 dB in power gain compared to CW operation. This improvement was achieved at elevated drain voltages (up to 18 volts) and indicated that the useable range of device drain voltage was extended in the pulsed mode.

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